EENG 5550 HW 1

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# Block diagram of Decoder 5 to 32

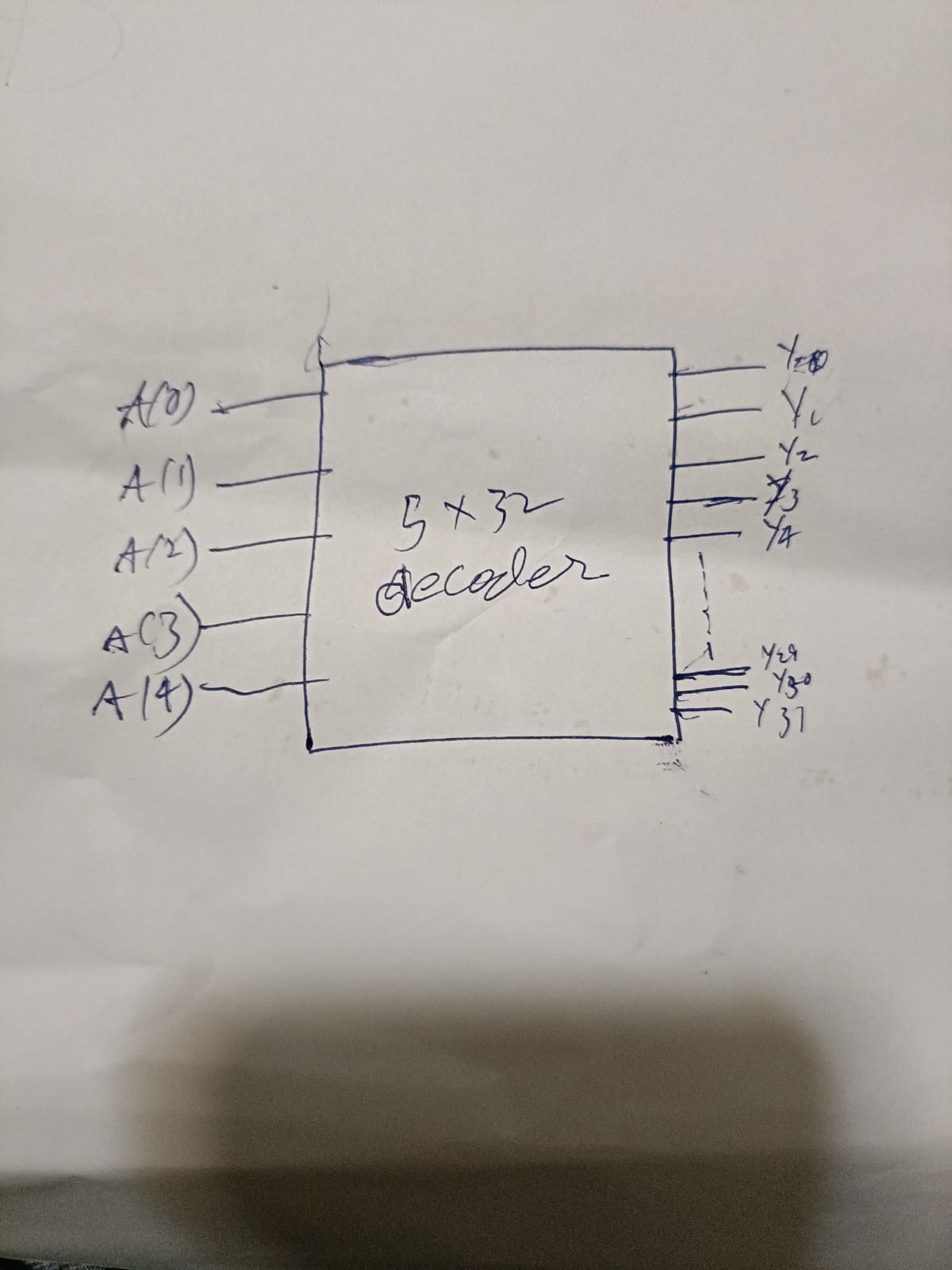


Figure Decoder 5 to 32

* Overall Component: Decoder 5 to 32
* Overall ports:
  + Inputs:
    - A
  + Outputs:
    - Z
* Subcomponents:
* Necessary intermediate signals:
  + A
  + Z

## Design\Algorithm ex:

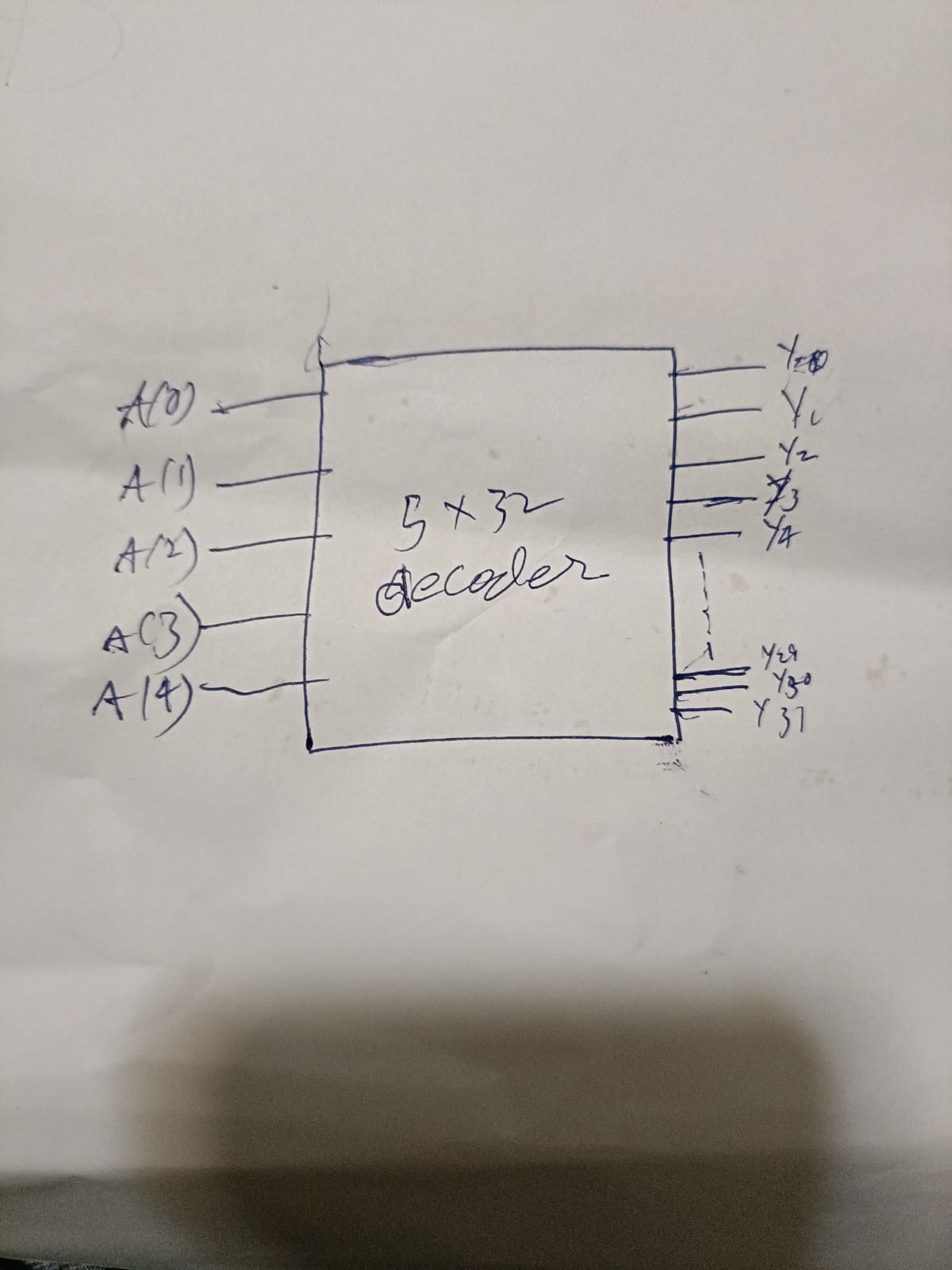


Figure 3 – 32 to 1 multiplexer

* Overall Component: Decoder 5\_32
* Overall ports:
  + Inputs:
    - A:
  + Outputs:
    - :Y single bit -> output

**Representation of design:**

|  |  |
| --- | --- |
| Select input | Resulting output |
| 00000 | 00000000000000000000000000000001 |
| 00001 | 00000000000000000000000000000010 |
| 00010 | 00000000000000000000000000000100 |
| 00011 | 00000000000000000000000000001000 |
| 00100 | 00000000000000000000000000010000 |
| 00101 | 00000000000000000000000000100000 |
| 00110 | 00000000000000000000000001000000 |
| 00111 | 00000000000000000000000010000000 |
| 01000 | 00000000000000000000000100000000 |
| 01001 | 00000000000000000000001000000000 |
| 01010 | 00000000000000000000010000000000 |
| 01011 | 00000000000000000000100000000000 |
| 01100 | 00000000000000000001000000000000 |
| 01101 | 00000000000000000010000000000000 |
| 01110 | 00000000000000000100000000000000 |
| 01111 | 00000000000000001000000000000000 |
| 10000 | 00000000000000010000000000000000 |
| 10001 | 00000000000000100000000000000000 |
| 10010 | 00000000000001000000000000000000 |
| 10011 | 00000000000010000000000000000000 |
| 10100 | 00000000000100000000000000000000 |
| 10101 | 00000000001000000000000000000000 |
| 10110 | 00000000010000000000000000000000 |
| 10111 | 00000000100000000000000000000000 |
| 11000 | 00000001000000000000000000000000 |
| 11001 | 00000010000000000000000000000000 |
| 11010 | 00000100000000000000000000000000 |
| 11011 | 00001000000000000000000000000000 |
| 11100 | 00010000000000000000000000000000 |
| 11101 | 00100000000000000000000000000000 |
| 11110 | 01000000000000000000000000000000 |
| 11111 | 10000000000000000000000000000000 |

# Generated RTL Block Diagram\Schematic

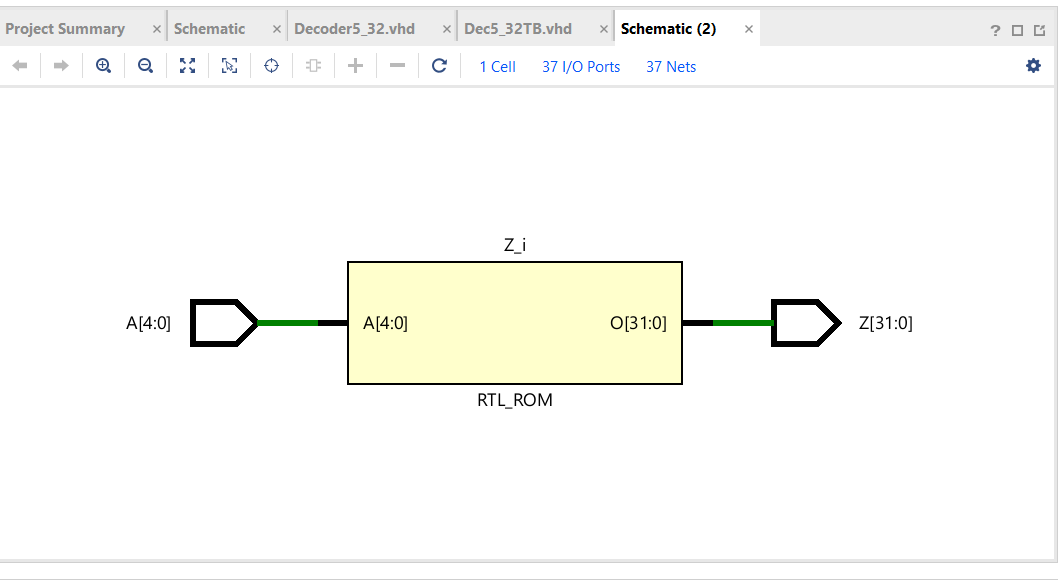


Figure 5 - generated RTL schematic.

# Results

## Waveforms

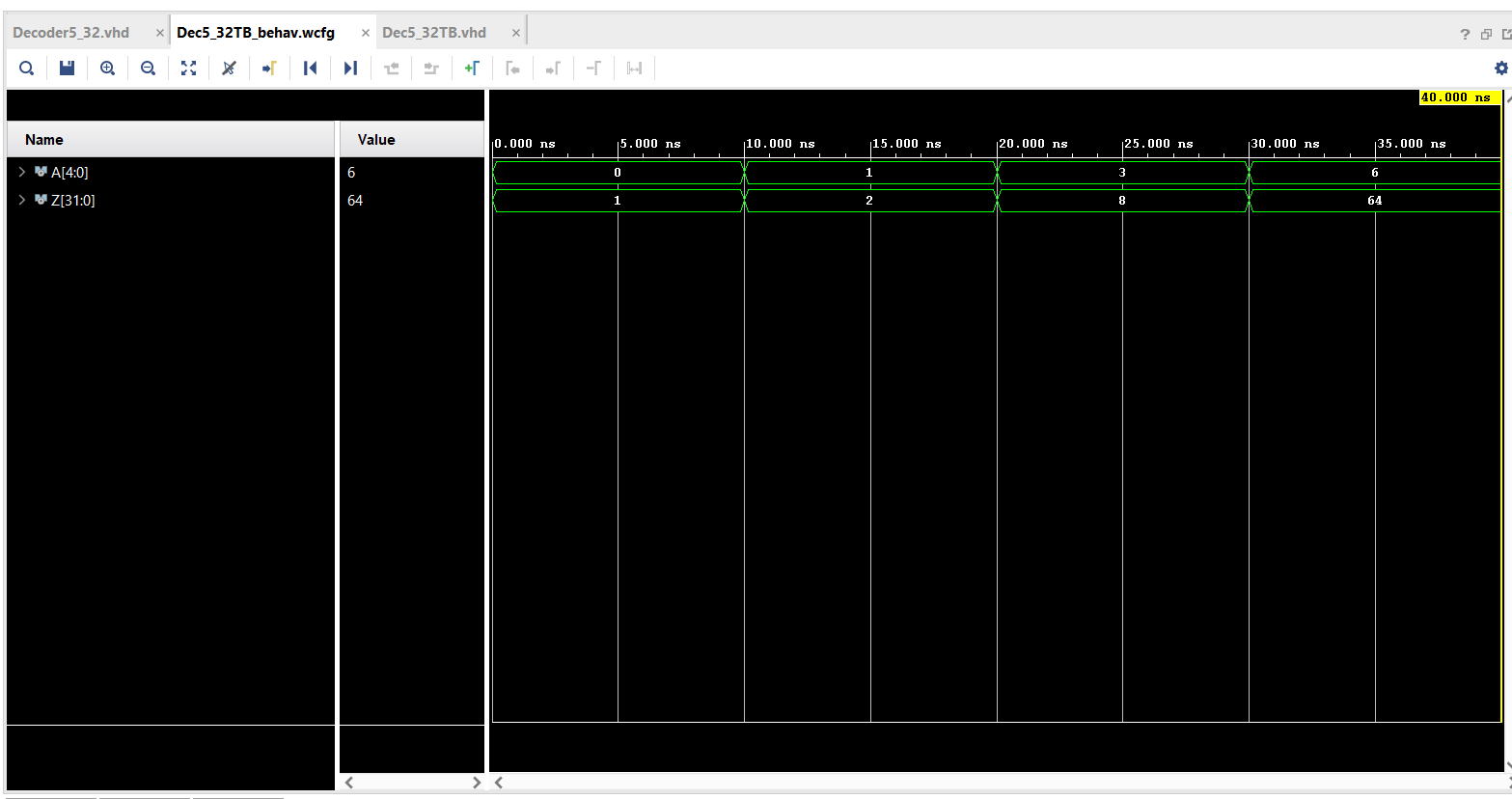


Figure 6 - Waveforms

## Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | calculations | waveforms |  |
|  | A | Y | Y | |
| Test case 1: | 0 | 1 | 1 | |
| Test case 2: | 6 | 64 | 64 | |